

REMARKS

The Office Action mailed July 21, 2003, has been carefully reviewed and by this Amendment, Applicant has canceled claims 2, 3 and 5-10 and amended claim 1. Claims 1 and 4 are pending in the application. In view of the amendments and the following remarks provided herein, favorable reconsideration and allowance of the application is respectfully requested.

The Examiner rejected claims 1-3, 7 and 10 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,326,696 to Horton et al. ("Horton"), and under 35 U.S.C. 103(a) rejected claim 4 as being unpatentable over Horton, claim 5 as being unpatentable over Horton in view of U.S. Patent No. 6,265,771 to Ference et al. ("Ference"), and claims 6, 8 and 9 as being unpatentable over Horton in view of U.S. Patent No. 6,326,696 to Chan et al. ("Chan").

As set forth in claim 1, which has been amended to incorporate the subject matter of claims 8 and 9, now canceled, the present invention is directed to a stack chip module including a substrate having a predetermined-size groove and a circuit pattern on each side, with one end of each circuit pattern being adjacent to a respective groove. The grooves are arranged on both sides of the substrate in a jig-jag form. A first semiconductor chip is adhered in each groove of the substrate by adhesive, with each of the first semiconductor chips having a plurality of center pads and a plurality of edge pads, electrically connected to each other, on an upper part of the respective first semiconductor chip. Gold wires electrically connect a respective circuit pattern of the substrate and the edge pads of a respective first semiconductor chip.

For each of the first semiconductor chips, as arranged in respective grooves on both sides of the substrate, a second semiconductor chip having a plurality of center pads

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corresponding to the plurality of center pads on the upper part of the respective first semiconductor chip and a formative side is arranged opposite to that of the respective first semiconductor chip. A plurality of bumps is interposed between the center pads of the first semiconductor chips and the center pads of the corresponding second semiconductor chips for joining and electrically connecting the respective center pads.

Horton does not disclose or suggest a substrate *having grooves in both sides thereof in a jig jag arrangement* for receiving first semiconductor chips which are electrically joined to respective second semiconductor chips through pads and bumps. While the Examiner has relied upon Chan for teaching the jig-jag arrangement as claimed, Chan does not in fact disclose *a substrate having grooves in both sides thereof, into which grooves* the first semiconductor chips are adhered, as claimed by the present invention and shown in Figure 9. Instead, Chan shows only a plurality of substrates 70 positioned in an offset arrangement from one another. This is not comparable to the *grooved unitary structure* shown and claimed by the present invention. Accordingly, Applicant respectfully requests reconsideration and allowance of claim 1 as amended

Claim 4 is also in condition for allowance as a claim properly dependent on an allowable base claim and for the subject matter set forth therein. Specifically, the prior art does not teach or suggest bumps having a height of 40 to 100 μ m to increase junction reliability (see the specification page 8, lines 13-16, and page 10, lines 3-5).

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Claims 2, 3 and 5-10 have been canceled to simplify the outstanding issues under consideration.

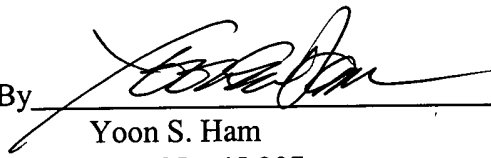
As the amendments set forth herein clarify the invention and place the application into condition for allowance, entry thereof is proper after Final action and is respectfully requested.

Should the Examiner have any questions or comments, the Examiner is cordially invited to telephone the undersigned attorney so that the present application can receive an early Notice of Allowance.

Respectfully submitted,

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